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claims 37-69 and 82-93.

All pending claims are reproduced below. Marked-up copies of the amended claims are provided in the Appendix to this Response.

1. A method of performing a design of an integrated circuit comprising:

defining a physical design of the circuit while tracking an error in prediction of a timing value associated with one or more nets in the circuit; and

determining a physical placement level of the circuit when the error in prediction of the timing value satisfies a predetermined threshold.

2. The method of claim 1, wherein the defining the physical design further comprises performing a soft placement of the design.

3. The method of claim 2, wherein the performing the soft placement of the design further comprises performing one or more of the following: placement of cells of the design, logic optimization of the design, routing of wires in the design, timing and clock control for the design and extraction of the design.

4. The method of claim 2, wherein the performing the soft placement of the design further comprises simultaneously performing one or more of the following in parallel: placement of cells of the design, logic optimization of the design, routing of wires in the design, timing and clock control for the design and extraction of the design.

5. The method of claim 1, wherein the determining the physical placement level of the circuit when the error in prediction of the timing value satisfies a predetermined threshold further comprises:

localizing placement of cells and wires in the physical design;

creating a profile of the wire lengths from the physical design;

calculating an error in a prediction of a timing value from the profile of the wire lengths; and

comparing the error in the prediction of the timing value with the predetermined threshold to determine if the error satisfies the predetermined threshold.

6. The method of claim 1, wherein the determining the physical placement level of the circuit when the error in prediction of the timing value satisfies a predetermined threshold further comprises:

(a) quadrisectioning the physical design into bins;

(b) localizing placement of cells and wires of the physical design into the bins;

(c) creating a profile of the wire lengths in each of the bins;

(d) calculating a plurality of errors in a prediction of timing values from the profile of the wire lengths for each bin respectively;

(e) comparing each of the plurality of errors in the prediction of the timing values with the predetermined threshold to determine if the error satisfies the predetermined threshold; and either:

further quadrisectioning the physical design and repeating (b through e); or

generating an interrupt if all of the plurality of errors in the prediction of the timing values for each of the bins satisfy the predetermined threshold.

7. The method of claim 6, wherein the creating of profile of the wire lengths in each of the bins further comprises plotting wire lengths versus instances of nets in each of the bins.

8. The method of claim 1, further comprising performing interactive optimization of the physical design after the error in prediction of the timing value satisfies the predetermined threshold.

9. The method of claim 1, further comprising analyzing one or more of the following characteristics of the physical design after the error in prediction of the timing value satisfies the predetermined threshold: congestion, timing, power, and signal integrity.

10. The method of claim 9, further comprising generating a report indicative of the congestion, timing, power, signal integrity of the physical design.

11. The method of claim 1, further comprising:

performing a second physical design of the circuit derived from the physical design of the circuit performed while tracking the error in prediction of the timing value associated with one or more nets in the circuit; and

generating a GDS file from the second physical design of the circuit.

12. The method of claim 11, wherein the performing the second physical design of the circuit further comprises simultaneously performing one or more of the following in parallel: placement of cells of the design, logic optimization of the design, routing of wires in the design, timing and clock control for the design and extraction of the design.

13. A computer-readable medium including computer code configured to perform the design of an integrated circuit, the computer code configures to effectuate the following:

defining a physical design of the circuit while tracking an error in prediction of a timing value associated with one or more nets in the circuit; and

determining a physical placement level of the circuit when the error in prediction of the timing value satisfies a predetermined threshold.

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14. (Once Amended) The computer-readable medium of claim 13, wherein the defining the physical design further comprises performing a soft placement of the design.

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15. (Once Amended) The computer-readable medium of claim 14, wherein the performing the soft placement of the design further comprises performing one or more of the following: placement of cells of the design, logic optimization of the design, routing of wires in the design, timing and clock control for the design and extraction of the design.

16. (Once Amended) The computer-readable medium of claim 14, wherein the performing the soft placement of the design further comprises simultaneously performing one or more of the following in parallel: placement of cells of the design, logic optimization of the

design, routing of wires in the design, timing and clock control for the design and extraction of the design.

17. (Once Amended) The computer-readable medium of claim 13, wherein the determining the physical placement level of the circuit when the error in prediction of the timing value satisfies a predetermined threshold further comprises:

localizing placement of cells and wires in the physical design;

creating a profile of the wire lengths from the physical design;

calculating an error in a prediction of timing value from the profile of the wire lengths; and

comparing the error in the prediction of the timing value with the predetermined threshold to determine if the error satisfies the predetermined threshold.

18. (Once Amended) The computer-readable medium of claim 13, wherein the determining the physical placement level of the circuit when the error in prediction of the timing value satisfies a predetermined threshold further comprises:

(a) quadrisectioning the physical design into bins;

(b) localizing placement of cells and wires of the physical design into the bins;

(c) creating a profile of the wire lengths in each of the bins;

(d) calculating a plurality of errors in a prediction of timing values from the profile of the wire lengths for each bin respectively;

(e) comparing each of the plurality of errors in the prediction of the timing values with the predetermined threshold to determine if the error satisfies the predetermined threshold; and either:

further quadrisectioning the physical design and repeating (b through e); or

generating an interrupt if all of the plurality of errors in the prediction of the timing values for each of the bins satisfy the predetermined threshold.

19. (Once Amended) The computer-readable medium of claim 18, wherein the creating of profile of the wire lengths in each of the bins further comprises plotting wire lengths versus instances of nets in each of the bins.

20. (Once Amended) The computer-readable medium of claim 13, wherein the computer code is further configured to effectuate performing interactive optimization of the physical design after the error in prediction of the timing value satisfies the predetermined threshold.

21. (Once Amended) The computer-readable medium of claim 13, wherein the computer code is further configured to effectuate analyzing one or more of the following characteristics of the physical design after the error in prediction of the timing value satisfies the predetermined threshold: congestion, timing, power, and signal integrity.

22. (Once Amended) The computer-readable medium of claim 21, wherein the computer code is further configured to effectuate generating a report indicative of the congestion, timing, power, signal integrity of the physical design.

23. (Once Amended) The computer-readable medium of claim 13, wherein the computer code is further configured to effectuate:

performing a second physical design of the circuit derived from the physical design of the circuit performed while tracking the error in prediction of the timing value associated with one or more nets in the circuit; and

generating a GDS file from the second physical design of the circuit.

24. (Once Amended) The computer-readable medium of claim 23, wherein the performing the second physical design of the circuit further comprises simultaneously performing one or more of the following in parallel: placement of cells of the design, logic optimization of the design, routing of wires in the design, timing and clock control for the design and extraction of the design.

25. A computer system configured to perform the design of an integrated circuit, the computer system comprising:

a physical design module configured to define a physical design of the circuit while tracking an error in prediction of a timing value associated with one or more nets in the circuit; and

a physical placement level module configured to determine a physical placement level of the circuit when the error in prediction of the timing value satisfies a predetermined threshold.

26. The computer system of claim 25, wherein the physical design module is further configured to perform a soft placement of the design.

27. The computer system of claim 26, wherein the physical design module is further configured to perform one or more of the following: placement of cells of the design, logic optimization of the design, routing of wires in the design, timing and clock control for the design and extraction of the design.

28. The computer system of claim 26, wherein the physical design module is further configured to simultaneously performing one or more of the following in parallel: placement of cells of the design, logic optimization of the design, routing of wires in the design, timing and clock control for the design and extraction of the design.

29. The computer system of claim 25, wherein the physical placement level module is configured to determine the physical placement level of the circuit when the error in prediction of the timing value satisfies a predetermined threshold by:

localizing placement of cells and wires in the physical design;

creating a profile of the wire lengths from the physical design;

calculating an error in a prediction of a timing value from the profile of the wire lengths; and

comparing the error in the prediction of the timing value with the predetermined threshold to determine if the error satisfies the predetermined threshold.

30. The computer system of claim 25, wherein the physical placement level module is configured to determine the physical placement level of the circuit when the error in prediction of the timing value satisfies a predetermined threshold by:

(a) quadrisectioning the physical design into bins;

(b) localizing placement of cells and wires of the physical design into the bins;

(c) creating a profile of the wire lengths in each of the bins;

(d) calculating a plurality of errors in a prediction of timing values from the profile of the wire lengths for each bin respectively;

(e) comparing each of the plurality of errors in the prediction of the timing values with the predetermined threshold to determine if the error satisfies the predetermined threshold; and either:

further quadrisectioning the physical design and repeating (b through e); or

generating an interrupt if all of the plurality of errors in the prediction of the timing values for each of the bins satisfy the predetermined threshold.

31. The computer system of claim 30, wherein the creating of profile of the wire lengths in each of the bins further comprises plotting wire lengths versus instances of nets in each of the bins.

32. The computer system of claim 25, further comprising a prototype optimization tool to optimize the physical design after the error in prediction of the timing value satisfies the predetermined threshold.

33. The computer system of claim 25, wherein the prototype optimization tool further comprises analyzing one or more of the following characteristics of the physical design after the error in prediction of the timing value satisfies the predetermined threshold: congestion, timing, power, and signal integrity.

34. The computer system of claim 33, further comprising a report generating tool configured to generate a report indicative of the congestion, timing, power, signal integrity of the physical design.

35. The computing system of claim 25, further comprising:

a second physical design tool configured to perform a second physical design of the circuit derived from the physical design of the circuit performed while tracking the error in prediction of the timing value associated with one or more nets in the circuit; and

a GDS tool configured to generate a GDS file from the second physical design of the circuit.

36. The computing system of claim 35, wherein the second physical design tool is configured to perform the second physical design of the circuit by simultaneously performing one or more of the following in parallel: placement of cells of the design, logic optimization of the design, routing of wires in the design, timing and clock control for the design and extraction of the design.

70. A method for a first party to fabricate a semiconductor device, comprising:

receiving an sign-off prototype, the sign-off prototype generated by:

defining a physical design of a circuit while tracking an error in prediction of a timing value associated with one or more nets in the circuit;

determining a physical placement level of the circuit when the error in prediction of the timing value satisfies a predetermined threshold; and

generating the sign-off prototype from the physical placement level of the circuit when the error in prediction of the timing value satisfies a predetermined threshold; and after receiving the sign-off prototype, the first party performing:

generating a second physical design of the circuit from the sign-off prototype;

generating a GDS file from the second physical design;

having a mask set generated from the GDS file; and

having the semiconductor device fabricated using the mask set.

71. The method of claim 70, wherein generating the second physical design of the circuit further comprises performing one or more of the following: placement of cells of the

design, logic optimization of the design, routing of wires in the design, timing and clock control for the design and extraction of the design.

72. The method of claim 71, wherein the performing the placement of cells of the design, logic optimization of the design, routing of wires in the design, timing and clock control for the design and extraction of the design occurs substantially in parallel using a physical design tool.

73. The method of claim 70, wherein the receiving the sign-off prototype further comprises receiving the sign-off prototype from a second party.

74. The method of claim 73, generating the second physical design of the circuit from the sign-off prototype further comprises having the second party to perform additional interactive optimization on the sign-off prototype after receiving the sign-off prototype so the second party can collaborate in resolving problems identified in the sign-off prototype.

75. The method of claim 70, wherein the determining the physical placement level of the circuit when the error in prediction of the timing value satisfies a predetermined threshold further comprises:

(a) quadrisectioning the physical design into bins;

(b) localizing placement of cells and wires of the physical design into the bins;

(c) creating a profile of the wire lengths in each of the bins;

(d) calculating a plurality of errors in a prediction of timing values from the profile of the wire lengths for each bin respectively;

(e) comparing each of the plurality of errors in the prediction of the timing values with the predetermined threshold to determine if the timing value satisfies the predetermined threshold; and either:

further quadrisectioning the physical design and repeating (b through e); or

generating an interrupt if all of the plurality of errors in the prediction of the timing values for each of the bins satisfy the predetermined threshold.

76. (Once Amended) A semiconductor device manufactured by a first party by:
receiving an sign-off prototype, the sign-off prototype generated by:

defining a physical design of a circuit while tracking an error in prediction of a timing value associated with one or more nets in the circuit;

determining a physical placement level of the circuit when the error in prediction of the timing value satisfies a predetermined threshold; and

generating the sign-off prototype from the physical placement level of the circuit when the error in prediction of the timing value satisfies a predetermined threshold; and

after receiving the sign-off prototype, the first party performing:

generating a second physical design of the circuit from the sign-off prototype;

generating a GDS file from the second physical design;

having a mask set generated from the GDS file; and

having the semiconductor device fabricated using the mask set.

77. The semiconductor device of claim 76, wherein generating the second physical design of the circuit further comprises performing one or more of the following: placement of cells of the design, logic optimization of the design, routing of wires in the design, timing and clock control for the design and extraction of the design.

78. The semiconductor device of claim 77, wherein the performing the placement of cells of the design, logic optimization of the design, routing of wires in the design, timing and clock control for the design and extraction of the design occurs substantially in parallel using a physical design tool.

79. The semiconductor device of claim 76, wherein the determining the physical placement level of the circuit when the error in prediction of the timing value satisfies a predetermined threshold further comprises:

(a) quadrisectioning the physical design into bins;

(b) localizing placement of cells and wires of the physical design into the bins;

(c) creating a profile of the wire lengths in each of the bins;

(d) calculating a plurality of errors in a prediction of timing values from the profile of the wire lengths for each bin respectively;

(e) comparing each of the plurality of errors in the prediction of the timing values with the predetermined threshold to determine if the timing value satisfies the predetermined threshold; and either:

further quadrisectioning the physical design and repeating (b through e); or

generating an interrupt if all of the plurality of errors in the prediction of the timing values for each of the bins satisfy the predetermined threshold.

80. The semiconductor device of claim 76, wherein the receiving the sign-off prototype further comprises receiving the sign-off prototype from a second party.

81. The semiconductor device of claim 80, wherein generating the second physical design of the circuit from the sign-off prototype further comprises having the third party to perform additional interactive optimization on the sign-off prototype after receiving the sign-off prototype so the second party can collaborate in resolving problems identified in the sign-off prototype.

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94. (Once Amended) A semiconductor device, comprising:

an integrated circuit segmented into a plurality of bins, the integrated circuit including:

a first bin having a first group of nets optimized to a first set of criteria; and

a second bin having a second group of nets optimized to a second set of criteria,

wherein the first criteria and the second criteria are substantially different.

95. The semiconductor device of claim 94, wherein the first bin is designed to a first GDS level and the second bin is designed to a second GDS level.

96. A computer-readable medium including computer code configured to perform the design of an integrated circuit, the computer code including:

timing and placement tools that are configured to generate a prototype, the timing and placement tools including:

a resource and allocation and sharing module;

an implementation module;

a logic structuring module;

a technology mapping module;

a global optimization module; and

a prototype optimization tool; and

a prototype optimization tool that enables the optimization of the prototype.

97. The computer readable medium of claim 96, further comprising a reporting tool configured to generate a report on design features defined by the prototype.

98. The computer readable medium of claim 96, wherein the resource and allocation and sharing module; the implementation module; the logic structuring module; the technology mapping module; the global optimization module; and the prototype optimization tool operate sequentially.

99. The computer readable medium of claim 96, wherein the resource and allocation and sharing module; the implementation module; the logic structuring module; the technology mapping module; the global optimization module; and the prototype optimization tool operate in parallel.

100. The computer readable medium of claim 96, wherein the timing and placement tools further comprise a logic optimization tool, a routing tool, a timing and clock analysis tool, and an extraction tool.